ABSTRACT OF THE DISCLOSURE

A method of generating a physical netlist for an integrated circuit design includes steps of: (a) receiving as input a representation of a core cell for a hierarchical integrated circuit design; (b) generating a physical netlist for a core cell model tile that maps logical ports of the core cell to physical ports of the core cell model tile; (c) including values for parasitic resistances connecting the logical ports of the core cell to the physical ports of the core cell model tile in the physical netlist for the core cell model tile; (d) connecting a hierarchical array of core cell model tiles so that the physical ports of each core cell model tile are connected to one another inside the array or mapped to an input/output port of the hierarchical array of core cell model tiles; and (e) generating as output a physical netlist of the hierarchical array of core cell model tiles.